Synchronizability of Distributed Clock Oscillators

Hisa-Aki Tanaka, Akio Hasegawa, Hiroyuki Mizuno, and Tetsuro Endo, *Senior Member, IEEE*

***Abstract*—We analyze the synchronizability of synchronous distributed oscillators (SDOs) [3], a novel clocking scheme for microprocessors. A computer-aided perturbation analysis is developed for such systems, where analytically tractable equations of the clock phases are reduced from experimental data reflecting all circuit details. Using this reduction, a theory is constructed to explain the underlying mechanism of the synchronization in SDOs. It systematically explains the observed phenomena, the existence and stability of the (mutually) synchronized states, and the transition from the in-phase synchronized state to the out-of-phase (but still synchronized) state. Furthermore, the present theory of phase reduction provides a new design principle of coupled oscillators based on "the equation"; a precise delay control (less than the gate delay) circuit can be designed in a simple and general form.**

***Index Terms*—Clock distribution network, impulse sensitive function, phase equation, ring oscillator, synchronization, voltage-controlled oscillator.**

I. Introduction

DIGITAL large-scale-integrated circuits (LSIs) are generally based on a synchronous scheme: a global clock signal acts as the "conductor of the orchestra," and each computing element acts as a "member of the orchestra," performing its operations synchronously at the command of the "conductor." Distribution of the clock signal in an LSI is thus an issue directly affecting the computing power of the LSI. However, the increasing size of circuits and rising clock frequencies are making it harder for only one "conductor" to distribute the clock signal (hereafter "the clock" for short) within an allowable phase error due to the skew and jitter. Clock networks using distributed voltage-controlled oscillators are good candidates for overcoming this difficulty because they can make multiple, mutually synchronized "conductors" that distribute the clock to all the "members" in unison [1]–[3]. Namely, this synchronous distributed oscillator (SDO) approach has advantages: it reduces skew and jitter coming from clock buffers and inter-line coupling in the conventional clock distribution approaches. Also, in [3], static jitter and skew caused by variation in the threshold voltage (as well as the supply voltage at one of the oscillators) is numerically investigated, where both jitter and skew are always reduced, compared to those in the conventional (noncoupled) multiple phase-locked loop (PLL) method. Although experimental data [2], [3] supports the feasibility of such distributed clock oscillators for high-performance circuits working at gigahertz frequencies, there is still insufficient understanding of the ability and limit of their synchronization. For this purpose, a general and practical theory of such distributed systems is required. However, in such experimental environments, even though synchronization phenomena can be observed clearly, neither the governing equation nor an analytically tractable model is available from the system, and this hampers theoretical insights into the synchronization.

Here, a method is developed to cope with such situations. We derive a set of simple equations for the clock phases, from experimental data reflecting all circuit details. This derivation is based on the phase response curve theory and the averaging method, which has been established in studies of nonlinear physics and mathematical biology [10]–[14]. What is new and important in the present study is the use of the experimental data about the phase response from the (weak) impulsive perturbations to the oscillating element. Such impulsive perturbation analysis has been recently devised in the insightful study by Hajimiri and Lee [4] on the phase noise in electrical oscillators. The present study, on the other hand, focuses on the effect of certain regular perturbations applied to the oscillator, rather than on statistical properties derived from random perturbation. The resulting phase equation of the clock explains the synchronization ability of SDOs and predicts the limit of synchronization due to signal delay and distortion. This prediction agrees with observations by Mizuno and Ishibashi [3], and it shows the validity of the phase reduction method for this system. The phase reduction method developed for SDOs can also be used as a design methodology for certain coupled oscillators; we can design a circuit of coupled oscillators from its phase equation with desired properties, and time-consuming exploration for circuits with circuit simulators can be eliminated.

In Section II, we briefly review the background and some observations for an SDO circuit. Section III introduces basic ideas and definitions required for the analysis of the system. In Section IV, a computer-aided impulsive perturbation analysis is developed for the phase equation of the system. As a natural consequence, a systematic explanation is obtained for the synchronization observed in SDOs. Furthermore, based on the phase equation, we are led to a new design methodology for coupled multiple oscillators; a precise phase resolution (less than the gate delay) generator is proposed as an example.

II. SDOs and Experimental Results

The core circuit of the SDO is simple: it consists of CMOS oscillators and wires interconnecting them (Fig. 1). The oscillators can be ring oscillators (ROs) or differential ring oscillators depending on the application.

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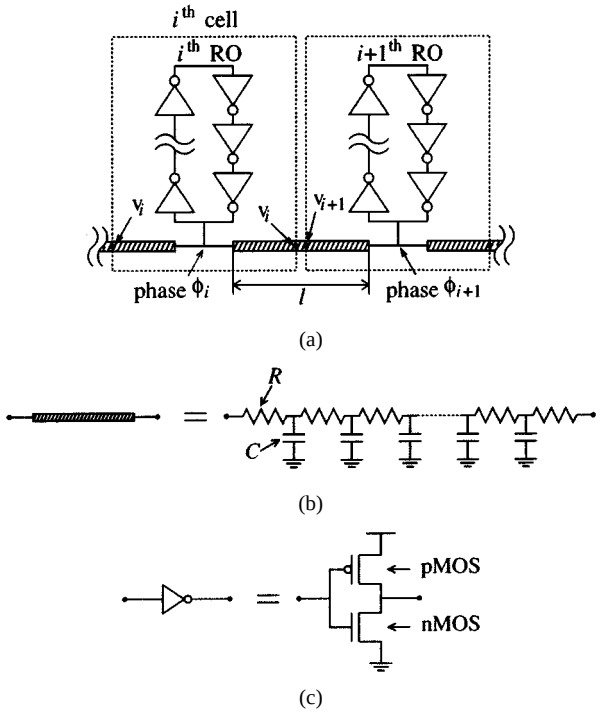


Fig. 1. (a) Core circuit of the SDO scheme in a linear array case. ROs are interconnected by wire. Each RO is a loop with an odd number of CMOS inverters. The dotted rectangles indicate the "cells" for which the sensitivity to weak impulsive perturbations was measured. (b) Wire modeled as an *RC* chain. (c) Inverter formed by a pair of pMOS and nMOS gates.

As shown in Fig. 1(a), such oscillators generally have an odd number of inverting devices (e.g., NOT-gates) in a closed loop. This creates an unstable state, resulting in robust oscillation with a rectangular waveform being used as the clock signal. Qualitatively, each inverting device can be roughly modeled as a switch (with a finite delay) that inverts a digital HIGH '1'/LOW '0' input to a LOW '0'/HIGH '1' output. However, modeling this with quantitative accuracy is not an easy task because each inverter is a highly nonlinear device, reflecting the physics of solid-state circuits. Here we consider an RO with a CMOS inverter [i.e., a pair consisting of a pMOS gate and an nMOS gate; see Fig. 1(c)], as used in the experiments of Mizuno and Ishibashi [3]. Semi-empirical models are used in the circuit simulator for the gates to reflect the measured characteristics of the devices (we used the LEVEL3 model in HSPICE [5], [6]), so a numerical transient analysis of the system can be done, taking into account the details of the gates. Mizuno and Ishibashi [3] used 0.25-μm CMOS gates in their simulations, but we used 1.6/1.2-μm (pMOS/nMOS) CMOS gates to make it easier to reproduce the simulation.

Also, the interconnection between oscillators is a dynamical system. In the simplest case, it can be modeled as a chain of resistors and capacitors [an *RC* chain shown in Fig. 1(b)] described by linear ordinary differential equations (ODEs). However, the interconnection between oscillators often includes multiple inverters for waveform regeneration, and nonlinear ODEs are required for this case. Thus, a precise description of the core circuit of the SDO requires a large number of lines of code in the circuit simulator, which can have an "`if then, else`" structure.

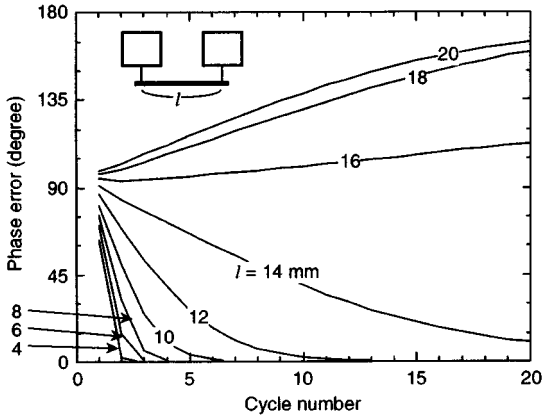


Fig. 2. Mizuno and Ishibashi numerically considered a linear array case for various values of l ($l = 4, \ldots, 20$ mm) (originally shown in [3]). The abscissa indicates the number of clock cycles (clock number) after two ROs initiate the oscillation with a 90° phase difference. The ordinate indicates the phase difference (phase error) between two ROs at each clock cycle. A transition between states was observed at $l_* = 14$ mm: below l_*, the phase difference tended to zero and above l_*, it tended to a constant. The change was observed to be sharp at around $l = l_*$. A 0.25-μm CMOS technology was used, and each 17-stage RO operated at around 600 MHz.

Thus, the detailed description of the circuit itself is quite complicated and far from analytically tractable. However, certain clear patterns of mutual synchronization were observed in the experiments done by Mizuno and Ishibashi (using a test chip operating at 200–400 MHz [3]). They also made systematic (transistor-level) circuit simulations to explore the synchronization ability of the SDOs. We followed their simulations (with different CMOS parameters as mentioned above) and obtained the same patterns of the mutual synchronization, which are summarized as follows.

1) The interaction between oscillators did not alter the original waveform in each (uncoupled) oscillating element [1]; the waveform itself was robust under the interaction.
2) Depending on the length of the wire $(\equiv l)$ between adjacent oscillators, the system showed two different stabilized states: complete synchronization with zero phase difference (for shorter l) and synchronization with a constant phase difference (for longer l) (Fig. 2).
3) The above two different synchronized states showed a sharp transition at a certain wire length l_* (Fig. 2).

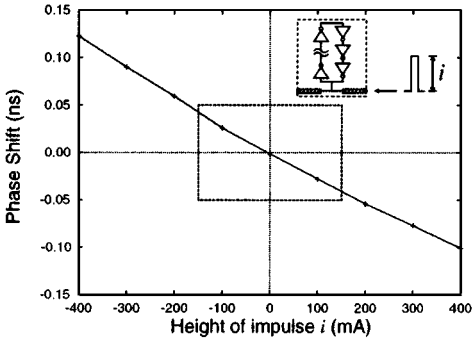
The mechanism underlying these phenomena will be clarified in Section IV.

III. Basic Ideas and Definitions

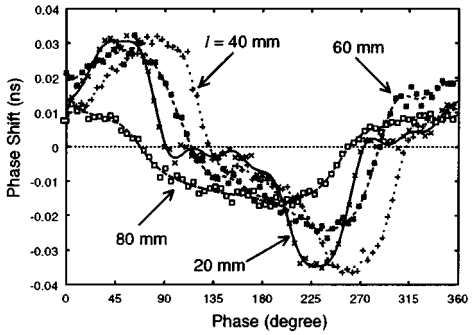
To make the description simpler, we focus on the case of a one-dimensional (1-D) SDO [Fig. 1(a)] here. This simplification is not essential and the same analysis can be made for any network topology.

While the system can be analyzed by dividing it into oscillators (ROs) and interconnections (wires), we use virtual "cells" [the dotted rectangles in Fig. 1(a)] to group oscillators and wires together. This simple idea turns out to be powerful; it enables

[1]Precisely, the oscillating element is a combination of the oscillator and the adjacent wires (defined as "cell" in Section III).



(a)



(b)

Fig. 3. Numerical data for cell shown in the inset. (a) Phase shifts (+) due to impulsive perturbations; the dotted rectangle in the center includes a LRR at the (fixed) rising part of the periodic waveform. (b) The impulse sensitivity $(\Gamma(\cdot) \cdot q_c)$ for four different wire lengths l. The abscissa indicates the phase (of one oscillation cycle) at which the impulse was injected. The ordinate indicates the amount of the phase shifted by the impulse. Four curves represent the interpolation of the impulse sensitivity (for $l = 20, 40, 60$, and 80 mm) using a Fourier series (ninth-order). The height of the injected impulse is 50 mA, and the charge displacement q_c is about 0.5 pC.

the following impulsive perturbation analysis and facilitates its extension to higher dimensional networks and to more complex interconnections having nonlinear effects.

Given a cell, we need information about its phase response to impulsive perturbations,[2] i.e.

1) the linear response region (LRR) [Fig. 3(a)];
2) the impulse sensitivity function (ISF) [Fig. 3(b)] defined in the LRR.

LRR and ISF are defined as follows. If we have a stable periodic oscillation, an impulsive perturbation (e.g., a current injection) can be applied at any phase (timing) of the one-cycle oscillation. The perturbed oscillator is pulled back to the original oscillation immediately after the impulse hits it, but a small phase shift (compared to the nonperturbed oscillator) remains. Thus, we can define a function of the phase shift with respect to the timing at which the impulse is applied, and this function is periodic with the period of the clock signal. We call it the ISF here. If we fix the timing of the perturbation, the amount of the phase shift is determined by the amount of the perturbation (the pulse height). For all the cases (of circuits, circuit parameters, and the timing of perturbation) that we considered, a linear relationship held between the phase shift and the pulse height, in a certain region around the zero pulse height [see the dotted central region in Fig. 3(a)]. We call this region with linear characteristics the linear response region, and it can be numerically (or experimentally) identified. Because of this linearity, the ISF is uniquely defined in the LRR. Interestingly, the ideas of ISF and LRR have been used in studies related to limit-cycle oscillators in nonlinear physics and theoretical biology [9]–[13]. In those cases, the ISF is commonly called the phase response curve (PRC), and the LRR is considered as the neighborhood of the limit-cycle where an isochrone (i.e., a manifold having the same phase) can be defined.

The notions of LRR and ISF for the voltage-controlled oscillator (VCO) are devised in the recent study of phase noise by Hajimiri and Lee. They first showed that a combination of circuit simulators and the notions of LRR and ISF provide a qualitatively and quantitatively powerful tool for jitter analysis and for designing VCOs with low jitter. More recently, Demir *et al.* presented a rigorous nonlinear analysis of phase noise based on the Floquet theory [14]. They pointed out that the (small) perturbation to the limit-cycle oscillator can be decomposed into the tangential direction of the limit-cycle and the subspace spanned by the remaining Floquet eigenvectors. Thus, for a weakly perturbed single VCO (limit-cycle oscillator), an experimental approach by Hajimiri and Lee and a mathematical foundation by Demir *et al.* is now established. Then, we are naturally led to the analysis of interacting multiple VCOs. In the next section, we consider the phase dynamics of the distributed, interacting VCOs.

IV. Phase Model and Its Implications

In an LSI, the interconnecting wires have high resistance (more than 100 Ω/cm), and the maximum current in them is so small (less than a few milliamperes) that the interacting oscillating elements in the SDO fall into the LRR. Here we consider the LRR and ISF of the virtual cell shown in Fig. 1(a). As discussed in Section III, the LRR is defined by the relationship between the injected impulse height and the phase shift of the oscillator in the cell, and the ISF $(\equiv\Gamma(\omega_0\tau))$ is defined by the timing of the impulse and the corresponding phase shift. Then, the (normalized) phase shift at time t (due to the unit impulse injected at time τ) is given by

$$h_\phi(t,\tau) = \frac{\Gamma(\omega_0\tau)}{q_{\max}} u(t-\tau) \tag{1}$$

where $q_{\max}$ is the maximum charge displacement across the capacitor on the node, $u(\cdot)$ is the unit step at $t=\tau$, and $\Gamma(\cdot)$ is the ISF, which has a period of $2\pi/\omega_0$.[3] Because each oscillator has a robust oscillation (a limit-cycle), the waveform of the oscillation (and the natural angular frequency ω_0) is robust under the weak interaction between oscillators. However, the instantaneous phase of each (ith) oscillator can be gradually shifted

[2]The system in this study is not linear time-invariant (LTI) and the relationship between the phase shift and the injected impulse height comes from the (local) structure of the limit-cycle oscillator (in other words, Floquet theory). Namely, the relationship between the phase shift and the injected impulse height is not given analytically as in the LTI case, but given numerically as follows.

[3]We used the same notation as in [4] for easier comparison between our theoretical results and those in [4]. In (1), $\Gamma(\omega_0\tau)$ is defined as the maximum phase shift (due to $q_{\max}$) at time τ.

by the perturbation, and this accumulated phase shift ϕ_i can be expressed by

$$\phi_i(t+t_d) = \int_{-\infty}^{t} h_\phi(t,\tau) i(\tau)\, d\tau \tag{2}$$

where $i(\tau)$ is the current injected into the cell and t_d is the (fixed) time delay for the injected impulse to reach the oscillator.[4] Thus, the phase ϕ_i is determined by the current $i(\tau)$. Conversely, this current $i(\tau)$ is determined by the interaction of the adjacent cells, the phases ϕ_i and ϕ_j $(j = i \pm 1)$ as follows. In each cell (ith cell), the oscillator has a robust waveform (i.e., the clock signal) and drives the voltages on the interconnecting wire. Then, the oscillating voltage v_i on the outer nodes of the ith cell is a certain function of the instantaneous oscillation phase of the oscillator: $\omega_0\tau + \phi_i$, as far as the oscillation is stable and the interconnection is fixed. It should be noted that the waveform v_i is not exactly the same as the clock signal on the oscillator, since the clock is delayed and distorted along the wire until it reaches the outer node. As the outer nodes of the cells are resistively connected, the current $i(\tau)$ (from the jth cell to the ith cell) is given by $R^{-1}(v_j - v_i)$, where R is the resistance between adjacent cells [Fig. 1(a)]. Then, (2) becomes

$$\phi_i(t+t_d) = \int_{-\infty}^{t} \frac{\Gamma(\omega_0\tau+\phi_i)}{q_{\max}R} \sum_{j=i\pm1} [v_j(\omega_0\tau+\phi_j) - v_i(\omega_0\tau+\phi_i)]\, d\tau \tag{3}$$

or equivalently

$$\frac{d\phi_i(t)}{dt} = \frac{\Gamma(\omega_0(t-t_d)+\phi_i(t-t_d))}{q_{\max}R} \times \sum_{j=i\pm1} [v_j(\omega_0(t-t_d)+\phi_j(t-t_d)) - v_i(\omega_0(t-t_d)+\phi_i(t-t_d))] \tag{4}$$

which implies that a closed relationship holds between ϕ_i and ϕ_j. By setting $\omega_0 t_d + \phi_{i,j}(t) - \phi_{i,j}(t-t_d) \equiv \psi_d$, we obtain

$$\frac{d\phi_i(t)}{dt} = \frac{\Gamma(\omega_0 t+\phi_i(t)-\psi_d)}{q_{\max}R} \sum_{j=i\pm1} [v_j(\omega_0 t+\phi_j(t)-\psi_d) - v_i(\omega_0 t+\phi_i(t)-\psi_d)]. \tag{5}$$

In (5), $i(\tau)(\equiv R^{-1}(v_j - v_i))$ is small (less than a few mA), and ω_0 is very large (several hundred megahertz–1 GHz); the time evolution of ϕ_i is much slower than that of $\omega_0 t$. This situation leads naturally to an application of the averaging method [6] [well-known in the ordinary differential (ODE) theory], where the slow motion of ϕ_i can be reduced by integrating $\Gamma(\omega_0\tau + \phi_i - \psi_d)\sum_{j=i\pm1}[v_j(\omega_0\tau+\phi_j-\psi_d) - v_i(\omega_0\tau+\phi_i-\psi_d)]$ with one cycle of $\omega_0\tau$. This integration can be handled by using the (numerically obtained) Fourier series of $\Gamma(\phi)$ and $v(\phi)$, which leads to the following form:

$$\oint \frac{\Gamma(\omega_0\tau+\phi_i-\psi_d)}{q_{\max}R} \sum_{j=i\pm1} [v_j(\omega_0\tau+\phi_j-\psi_d) - v_i(\omega_0\tau+\phi_i-\psi_d)]\, d\tau \equiv \Omega_i + H_i(\phi_{i+1}-\phi_i, \phi_{i-1}-\phi_i) \tag{6}$$

[4]In [4], this time delay is assumed to be 0, because the impulse is applied directly to the oscillator.

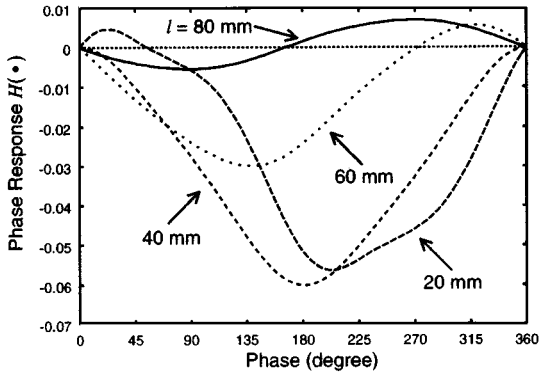


Fig. 4. Nonlinear phase characteristics ($H(\cdot)$ in (8)) for different wire lengths. All curves pass through zero. The slope at zero is positive for $l = 20$ mm, nearly zero but still positive for $l = 40$, and negative for $l = 60$ and 80 mm.

and

$$\dot{\phi}_i = \Omega_i + H_i(\phi_{i+1}-\phi_i, \phi_{i-1}-\phi_i) \tag{7}$$

where Ω_i is a (small) frequency deviation from the synchronized frequency ($\sim\omega_0$); this frequency deviation comes from the interaction (perturbation) effect as well as the threshold voltage and the supply voltage variation. Process variation may possibly affect the shape of H_i slightly. However, as we will see, introducing a small variation in H_i as well as Ω_i does not alter the system's synchronization ability.

As in (6), computing H_i requires Γ and $v_j - v_i$. Although Γ has been defined by the maximum charge displacement $q_{\max}$, the exact value of $q_{\max}$ is not necessarily needed for computing H_i. Instead of $q_{\max}$, we considered a fixed charge displacement q_c ($<q_{\max}$ that corresponds to the pulse size) and systematically obtained the phase shift for different cases as in Fig. 6 (later). It should be noted that the time delay t_d of the impulse (the phase delay ψ_d) vanishes in (6) and (7). However, $\Gamma(\phi)$ and $v_{i,j}(\phi)$ contain information about the effects of the time delay, and the shape of H_i reflects the signal delay and distortion.

A. Synchronization Limit of the SDO

In the 1-D linear SDO, the interconnecting wire (*RC* chain) has a symmetric bidirectional nature, and the currents $i(\tau)$ from both (left and right) adjacent cells do not interact with each other. Thus, for this particular case, the phase equation (7) takes the following form:

$$\dot{\phi}_i = \Omega_i + H(\phi_{i+1}-\phi_i) + H(\phi_{i-1}-\phi_i). \tag{8}$$

As shown in Fig. 4, the form of H strongly depends on wire length l. Although $H(0) = 0$ holds for any wire length (the in-phase state always exists, see Appendix I), the slope at $H(0)$ can be positive or negative. For wire lengths less than 40 mm, this slope is positive, and for longer cases ($l = 60, 80$ mm), it becomes negative and another zero crossing point appears as shown in Fig. 4.

In Mizuno and Ishibashi's study [3], the global effect of V_t variation (as well as supply voltage variation) at one of the oscillators is numerically investigated, where it is observed that the static skew is proportional to V_t deviation. The static skew is the phase difference between oscillators and it corresponds to

$\phi_{i+1} - \phi_i$ $(=\phi_i - \phi_{i-1})$ in (8). Also, the natural frequency deviation Ω_i is proportional to V_t deviation. From (8), it is clear that the static skew $\phi_{i+1} - \phi_i$ is proportional to Ω_i if the oscillators are mutually synchronized $(; \phi_i = 0)$. Thus, the presented theory is consistent to the observation in [3] regarding the effect of V_t deviation.

If we consider a 1-D circular network of SDO, a synchronized state with uniform phase differences: $\phi_{i+1} - \phi_i \equiv \phi_o$ $(i = 1, \ldots, N)$ with $N\phi_o = m \cdot 2\pi$ (m: integer) is possible. For such a solution of (7), linear stability theory proves that for positive $H'(\pm\phi_o)$ the synchronized state is stable and for negative $H'(\pm\phi_o)$ it becomes unstable (see Appendix II). For example, let's consider circular SDOs with five or six (an odd or even number of) oscillators. Numerical simulations (with HSPICE) show that, for $l < 40$ mm, only in-phase synchronized states $(\phi_o = 0)$ are observed for both cases. This can be explained theoretically as follows: for $\phi_o = 0, H(0) = 0, H'(0) > 0$, and $\Omega_i = 0$ implies that this state is stable. On the other hand, for a (formal) solution with $\phi_o \neq 0$, a certain amount of the frequency deviation Ω_i is required because $0 = \Omega_i + H(\phi_o) + H(-\phi_o)$ must be satisfied. However, Ω_i is restricted to some small range around $\Omega_i = 0$ because in ROs the oscillation period is proportional to the gate delay of each invertor and this cannot be altered much by the weak interaction due to $i(\tau)$. Then, such a phase-lagged solution is not realized. Thus, the in-phase solution with $\phi_o = 0$ is the only stable state for the shorter wire case.

In contrast to the shorter wire case, for larger l (>40 mm), only phase-lagged synchronized states $(\phi_o = \pi)$ are observed numerically for the case of $N = 6$. Although the in-phase state is possible ($H(0) = 0$, as shown in Fig. 4), the slope of $H'(0)$ is negative and this implies that the in-phase state is unstable and cannot be realized. On the other hand, the phase-lagged (anti-phase) state with $\phi_o = \pi$ is realized for the case of $N = 6$, because $H'(\pm\phi_o)$ are positive, and $H(\cdot)$ has a zero crossing point close to $\phi_0 = \pi$ and $H(\phi_o) + H(-\phi_o)$ becomes small (as observed in the case of 80 mm in Fig. 4). For the case of $N = 5$, the phase-lagged state with $\phi_0 \sim \pi$ does not exist, and neither the in-phase nor the phase-lagged synchronized states are observed.

As we have observed, there is a critical length l_* (~40 mm) between the stable in-phase state and the phase-lagged state, at which $H'(0) = 0$ holds. This critical length is unpractically large for the CMOS parameters we considered. However, it scales down as the CMOS gates are scaled. As shown in Fig. 2, l_* is around 14 mm for 0.25-μm CMOS parameters (with an operating frequency of around 600 MHz), where the value of l_* is in the "practical" range. Although we have chosen a particular parameter set for the computer-assisted derivation of the phase models, the predicted in-phase to phase-lagged state transition does not depend on a particular set of parameters. Our theory thus agrees with Mizuno and Ishibashi's results [3]. Although the shape of $H(\cdot)$ gradually approaches a sinusoidal wave as l becomes larger, the position of the O (on these curves) is observed to gradually shift to the right as l becomes larger. This can be understood by the fact that $\Gamma(\cdot)$ and $v_{i,j}$ reflect the internal delay of the cell and this delay is mapped to the phase shift of $H(\cdot)$. Thus, the emergence of the phase-lagged synchronized state can be explained by the deformation of $H(\cdot)$, and the underlying mechanism of a sharp transition at l_* (but still supposed to be continuous) is clarified.

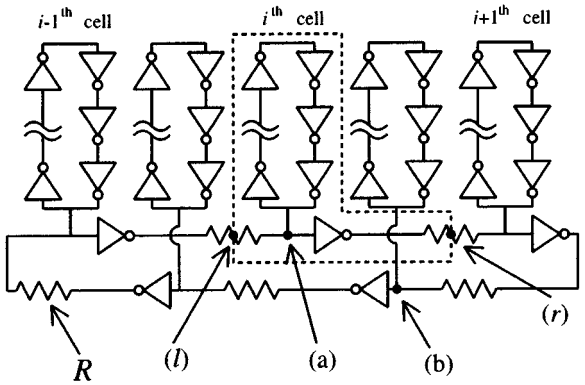


Fig. 5. Core circuit of CPG-like circuit incorporating the asymmetric interaction of adjacent oscillators. The dotted area defines a cell. Instead of a long wire between oscillators, resistor R is inserted. In the steady state, adjacent nodes show rectangular voltage waveforms with phase difference of $\pi - \pi/M$ radian. Because the oscillation frequency is nearly the same as that in a single (uncoupled) RO, a precise delay of $\tau_{\rm gate}/M$ can be obtained at nodes (a) and (b).

The above predictions guarantee the correct function of the SDO for $l < l_*$, that is, there is a unique, stable, in-phase state. The theory also predicts that a limit of the SDO appears at l_*. Beyond l_*, there is no stable in-phase state, which means that the SDO no longer provides correct synchronous clocking for LSIs. Although we have not proved that l_* matches half the wavelength of the clock signal on the wire, we do have numerical evidence for it. Therefore, for the SDO to function correctly, the wire length should be shorter than a certain length, which is thought to be inversely proportional to the clock frequency, that is, there is an upper limit on the operating frequency in the SDO.

B. Novel Circuit Design

Having obtained a method for reducing the interacting oscillators into a set of equations in terms of the phases, it is now possible to design and analyze circuits based on "the equation." We consider here a precise delay generating circuit as a practical example. In a single RO, the delay resolution (minimum phase difference between two voltage signals on the nodes) is bounded by a single gate delay $(\equiv\tau_{\rm gate})$. However, if multiple (M) ROs are coupled in a certain manner, the delay resolution can be of the order of $\tau_{\rm gate}/M$. In the previous (and first) circuit proposed for this purpose, special 2-input, 1-output buffers (instead of usual CMOS inverters) were developed, and the resulting circuit had two-dimenisonal network topology with many interconnections [8]. Their circuit seems beautiful and somewhat ingenious. However, a question arises: if certain good oscillators (in particular, ones having noise immunity) are available, is it not possible to achieve the function by simply interconnecting those oscillators (instead of developing a special buffer)?

Based on "the equation" discussed above and an analogy to the central pattern generator (CPG) circuit [11], a simpler and general formulation of circuits is possible, where the network topology is 1-D (fewer interconnections), and each oscillator can be any type of oscillator (in practice, noise immunity is essential). As a realization of the above idea, we consider here the simplest case, i.e., ROs and one inverter on the wire (Fig. 5). The cell can be defined as in Fig. 5. For this choice of the cell, we have checked that the voltage waveforms at nodes (l), (a), and (r) in the isolated cell (see

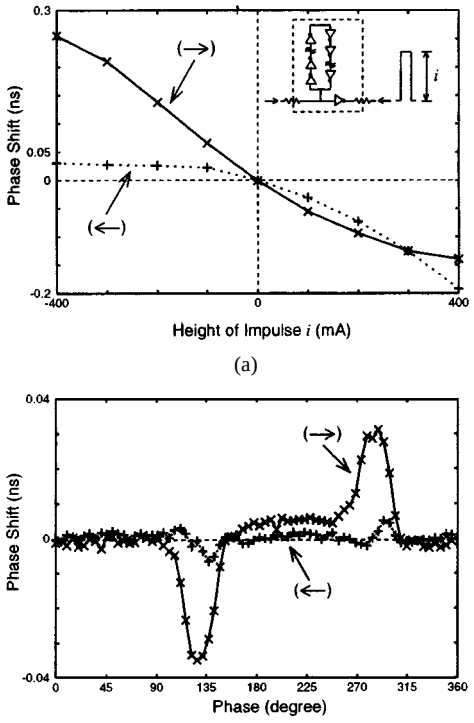


Fig. 6. Numerical data for cell shown in the inset. (a) Phase shifts due to impulsive perturbations; the injection from the left node (→) and the right node (←) are measured separately. (b) The impulse sensitivity ($\Gamma(\cdot) \cdot q_c$) for both directions; impulse from the left node (→) and right node (←). The impulse height is 50 mA, and the charge displacement q_c is about 0.5 pC.

Fig. 5) coincide with those in the full system (when the cells are interconnected). Thus, this choice of cell is well defined. In contrast to the symmetric interaction in the SDO, in this CPG-like circuit, the interaction is highly asymmetric; the LRR and ISF must be defined separately for the impulses from the left and right directions. Then, the phase equation for this system takes the following form:

$$\frac{d\phi_i}{dt} = \Omega_i + H_{\text{left}}(\phi_{i-1} - \phi_i) + H_{\text{right}}(\phi_{i+1} - \phi_i), \quad i = 1, \ldots, N. \quad (9)$$

In (9), unlike (8) for the SDO, the effect $H_{\text{left}}(\cdot)$ from the left $(i-1)$th cell dominates and $H_{\text{right}}(\cdot)$ from the right $(i+1)$th) cell is negligible, because the phase shift is negligible for any timing of the perturbation from the node (r). $H_{\text{left}}(\cdot)$ has multi-modal characteristics and there are two zero crossing points ϕ_o $(=\phi_{i-1} - \phi_i)$ as shown in Fig. 7; one is very close to π (this is analytically obtained in Appendix I). At this point, the slope $H'(\cdot)$ is negative, and the other one is close to π and $\phi_o < \pi$ and here $H'(\cdot)$ is positive and ϕ_o can be close to $\pi - \pi/N$ for a certain N. This implies that $H_{\text{left}}(\pi - \pi/N) \sim 0$ in (9), so the phase-lagged state $\phi_o = \pi - \pi/N$ is the only stable synchronized state (see Appendix II). Numerical simulation of this system verifies this prediction (as shown in Fig. 8 for the $N = 5$ case).

Thus, a difference between our CPG-like circuit and the SDO can be clarified from their phase equations (8) and (9). For the CPG-like circuit in Fig. 5, the phase-lagged state (uniform phase difference of π/M radian) is the only stable state, as opposed to the in-phase state (no phase difference) for the SDO. This prediction was verified using HSPICE under the same simulation

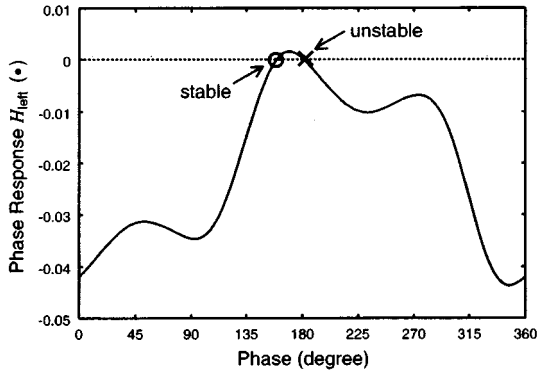


Fig. 7. Nonlinear phase characteristics ($H_{\text{left}}(\cdot)$ in (9)) with resistance $R = 100\ \Omega$.

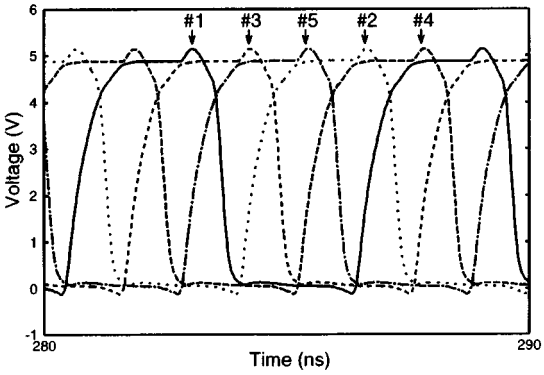


Fig. 8. Oscillation waveforms in the CPG-like circuit (Fig. 5), having five coupled (15-stage) ROs.

protocol used in the above SDO case (Fig. 8), including the simulation in a slightly noisy environment.

V. Conclusion

This study has presented a computer-aided phase reduction method for coupled oscillators; the SDO. The method is based on the fact that the oscillators interact weakly in a practical situation on an LSI chip, and on the use of the ISF (or PRC) from experimental data. Explicit dynamical phase equations for ROs and coupled ROs can be derived in the first place, which enables theoretical insights into their synchronization ability as well as synchronization limit. The presented phase reduction has general applicability, and this benefits an "equation-based" design of coupled oscillator systems that have a simple and general structure.

Appendix I
Analytical Description of the Phase Comparison Characteristics $H(\cdot)$

This appendix shows an analytical approach to describe some properties of $H(\cdot)$: a zero crossing point of $H(\cdot)$ and the slope of $H(\cdot)$ at that point.

From the definition (6), the phase comparison characteristics $H(\phi_j - \phi_i)$ can be determined by $v_{i,j}$ and Γ. For the 1-D SDO, the waveforms of v_i and v_j are exactly the same and can be given by

$$v_{i,j}(\tau) = \sum_{k=0} [a_k \cos k\theta_{i,j} + b_k \sin k\theta_{i,j}] \quad (10)$$

and the corresponding ISF becomes

$$\Gamma(\phi_i) = \sum_{k=0}[\alpha_k \cos k\theta_i + \beta_k \sin k\theta_i] \tag{11}$$

with $\theta_{i,j} = \omega_0\tau + \phi_{i,j} - \psi_d$. Then, $H(\cdot)$ is obtained as

$$\begin{aligned} H(\phi_j - \phi_i) \sim (1/2)\sum_{k=0}[&-(a_k\alpha_k + b_k\beta_k) + (a_k\alpha_k + b_k\beta_k) \\ &\times \cos k(\phi_j - \phi_i) + (-a_k\beta_k + b_k\alpha_k) \\ &\times \sin k(\phi_j - \phi_i)]. \end{aligned} \tag{12}$$

From (12), we have $H(0) = (1/2)\sum_{k=0}[-(a_k\alpha_k + b_k\beta_k) + (a_k\alpha_k + b_k\beta_k)] = 0$, which explains why all phase comparison characteristics $H(\cdot)$ in Fig. 4 (obtained from the experimental data of the ISFs) pass the O.

For the CPG-like circuit, the waveforms of $v_{i,j}$ are slightly different and the phase shift π due to the inverter should be taken into account as follows:

$$v_i(\tau) = \sum_{k=0}[a_k \cos k\theta_i + b_k \sin k\theta_i] \tag{13}$$

and

$$v_j(\tau) = \sum_{k=0}[\widehat{a_k} \cos k\theta_j + \widehat{b_k} \sin k\theta_j] \tag{14}$$

with $\theta_i = \omega_0\tau + \phi_i - \psi_d$, $\theta_j = \omega_0\tau + \phi_j + \pi - \psi_d$. Then we have

$$\begin{aligned} H(\phi_j - \phi_i) \sim (1/2)\sum_{k=0}[&-(a_k\alpha_k + b_k\beta_k) + (\widehat{a_k}\alpha_k + \widehat{b_k}\beta_k) \\ &\times \cos k(\phi_j - \phi_i + \pi) + (-\widehat{a_k}\beta_k + \widehat{b_k}\alpha_k) \\ &\times \sin k(\phi_j - \phi_i + \pi)]. \end{aligned} \tag{15}$$

If $a_k = \widehat{a_k}$ and $b_k = \widehat{b_k}$, then $H(\pi) = 0$ holds. However, as a_k and $\widehat{a_k}$, and b_k and $\widehat{b_k}$ are slightly different, the zero crossing point of (15) is slightly shifted from π. This explains why the zero crossing point in the experimental data is close to π, as shown in Fig. 7.

Now we consider the situation where a "cell" (defined in Section III) is perturbed by an external impulse. For this cell, a limit cycle $\vec{X}$ is defined in the (high-dimensional) state space and the external impulse is given by a perturbation vector $\Delta\vec{X}$ at some point of the limit cycle $\vec{X}$. In the neighborhood of $\vec{X}$, a local coordinate is given by the tangential direction of $\vec{X}$ and the "isochrone: which defines the phase ϕ of the oscillation. On this coordinate, the perturbation $\Delta\vec{X}$ is decomposed into two elements: one is tangential to $\vec{X}$ and the remaining is tangential to the isochrone. In the present situation we consider, the limit cycle is strongly attractive and the remaining element dies out immediately (after a signal delay t_d in the cell). It is noted that the tangential direction of $\vec{X}$ is not necessarily orthogonal to the isochrone. (A simple model is analyzed to consider this nature in [15].) However, if this orthogonality is satisfied (at least approximately), a great deal of simplification can be made in the expression of $H(\cdot)$. Here we will consider such a hypothetical situation and see what can be concluded.

If the orthogonality is assumed, the phase shift $\Delta\phi$ (due to $\Delta\vec{X}$) is simply given by

$$\Delta\phi = \frac{2\pi}{T}\left(\Delta\vec{X} \cdot \frac{\dot{\vec{X}}}{|\dot{\vec{X}}|^2}\right) \tag{16}$$

where $\dot{\vec{X}}$ denotes the time derivative of $\vec{X}$ and it is tangential to $\vec{X}$. If we consider the situation where the state variables are node voltages and an impulse is applied to the ith node, then $\vec{X}, \Delta\vec{X}$, and $\dot{\vec{X}}$ are respectively given as $\vec{X} = [v^{(1)}, \ldots, v^{(i)}, \ldots, v^{(n)}]$, $\Delta\vec{X} = [0, \ldots, 0, \Delta v^{(i)}, 0, \ldots, 0]$, and $\dot{\vec{X}} = \vec{X}' = (2\pi/T)[v^{(1)'}, \ldots, v^{(i)'}, \ldots, v^{(n)'}]$, where $\vec{X}'$ denotes the derivative with respect to phase ϕ. Then, the phase shift (16) becomes

$$\Delta\phi = \Delta v^{(i)} \frac{v^{(i)'}}{\sum_{i=1}^{n}\left(v^{(i)'}\right)^2}. \tag{17}$$

By the definition of the ISF in (1), $v^{(i)'}/\sum_{i=1}^{n}(v^{(i)'})^2$ corresponds to $\Gamma(\phi)$.

In our particular examples (1-D SDO and CPG-like circuit), $\Delta v^{(i)}$ corresponds to the interaction of the adjacent cells; $\Delta v^{(i)} = v_j^{(i)} - v_i^{(i)}$. It should be noted that the cell in these cases is spatially extended and the denominator $\sum_{i=1}^{n}(v^{(i)'})^2$ contains information about the signal delay due to the spatially extended interconnections.

If the denominator $\sum_{i=1}^{n}(v^{(i)'})^2$ is a constant, then $\Gamma(\phi_i) \sim v_i'(\phi_i)$ holds, so $H(\phi_j - \phi_i) \sim (1/2)\sum_{k=0}[({a_k}^2 + {b_k}^2)k \sin k(\phi_j - \phi_i)]$ and $H'(0) > 0$ is obtained. This implies that the phase comparison characteristics are an odd function and do not match the experimental data shown in Fig. 4. Here, the above insight that $\sum_{i=1}^{n}(v^{(i)'})^2$ reflects the spatially extended nature of the cell is essential to explain the characteristics of $H(\cdot)$. This insight and (12) predict that the slope $H'(0)$ is positive for shorter wire lengths (where $\sum_{i=1}^{n}(v^{(i)'})^2$ can be considered to be nearly a constant and $\Gamma(\phi_i) \sim v_i'(\phi_i)$) and $H'(0)$ can be negative for longer wire lengths because $\sum_{i=1}^{n}(v^{(i)'})^2$ reflects a larger signal delay in the cell and deviates from a constant. This prediction is consistent with the experimental data in Fig. 4 where $H'(0)$ changes from positive to negative as the wire length l becomes larger.

APPENDIX II

This appendix shows a criterion for the linear stability of the mutually synchronized states. We assume a synchronized state $\phi_{i+1} - \phi_i = \phi_o$ ($N\phi_o = m \cdot 2\pi$) and introduce a small perturbation δ_i to ϕ_i such that $\widehat{\phi_i} \equiv \phi_i + \delta_i$. Then, (8) becomes

$$\begin{aligned} \dot{\phi}_i + \dot{\delta}_i &= \Omega_i + H(\widehat{\phi_{i+1}} - \widehat{\phi_i}) + H(\widehat{\phi_{i-1}} - \widehat{\phi_i}) \\ &= \Omega_i + H(\phi_o) + H(-\phi_o) + H'(\phi_o)(\delta_{i+1} - \delta_i) \\ &\quad + H'(-\phi_o)(\delta_{i-1} - \delta_i) + O(\delta^2). \end{aligned} \tag{18}$$

After removing the synchronized part in (18), we obtain the linear ODE for δ_i as

$$\begin{pmatrix} \dot{\delta}_1 \\ \vdots \\ \dot{\delta}_i \\ \vdots \\ \dot{\delta}_N \end{pmatrix} = (a+b) \begin{pmatrix} -1 & s & 0 & \cdots & 0 & r \\ r & -1 & s & \cdots & 0 & 0 \\ 0 & r & -1 & s & \cdots & 0 \\ \vdots & \ddots & \ddots & \ddots & \ddots & s \\ s & 0 & \cdots & 0 & r & -1 \end{pmatrix} \begin{pmatrix} \delta_1 \\ \vdots \\ \delta_i \\ \vdots \\ \delta_N \end{pmatrix} \tag{19}$$

in which $r = a/(a+b), s = b/(a+b), a = H'(\phi_o)$, and $b = H'(-\phi_o)$. The matrix in (19) is known as a circulant matrix and

its eigenvalues λ_k and eigenvectors e_k can be explicitly obtained as

$$\lambda_k = r\exp(2\pi ik/N) + s\exp(-2\pi ik/N) - 1$$
$$e_k = [\exp(-2\pi ik/N), \ldots, \exp(-2\pi ikj/N), \ldots, \exp(-2\pi ikN/N)], \qquad k = 1, \ldots, N. \tag{20}$$

Then, $\mathrm{Re}\{\lambda_k\} \leq 0$ holds for any a, b, and k, and the stability of the synchronized states can be determined by $(a+b)$ in (19). For the in-phase state with $H'(0) > 0$, $(a+b) = 2H'(0) > 0$ and $\mathrm{Re}\{\lambda_k\} \leq 0$ implies it is stable, and for $H'(0) < 0$ it is unstable. Also, if the phase-lagged synchronized state satisfies $a + b = H'(\phi_o) + H'(-\phi_o) > 0\ (< 0)$, then it is stable (unstable). The same analysis can be made for the stability for (9). If the $H_{\mathrm{right}}(\cdot)$ term in (9) is neglected, the linear ODE for the perturbation δ_i is obtained from (19) by setting $a = 0$, and the same stability criterion is obtained. For $H'_{\mathrm{left}}(\phi_o) > 0$ the synchronized state is stable and for $H'_{\mathrm{left}}(\phi_o) < 0$, it is unstable.

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