linear gradient error in the DAC. This corresponds to a midrange error of 0.4%. Finite (54dB) DC gain for all opamps and randomly mismatched capacitors (with 0.1% standard deviation) were assumed in all circuits. OSR = 4 was used. A 0.45V peak midband two-tone input signal u_1 was applied to DS_1, and a second-order single-bit ΔΣ ADC realised DS_2. To demonstrate the high linearity achievable with the proposed correction, DS_1 was embedded in a 2-0 MASH containing a 10 bit ADC as its second stage. The mismatch between the MASH stages was not considered; it can also be corrected by digital methods [9].

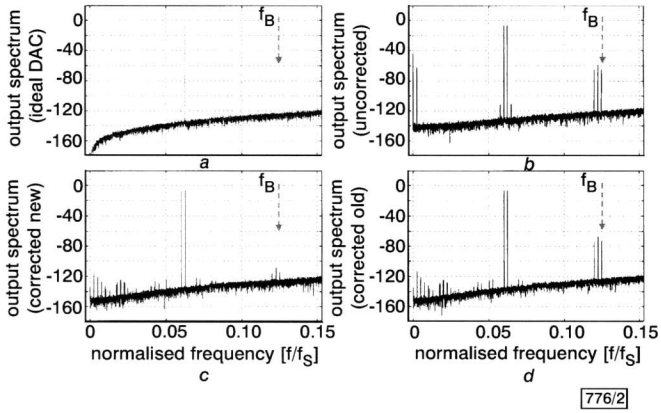

Fig. 2 *Output spectra of MASH (computed using 64× averaged FFTs for 2^{15} samples)*

a For ideal DAC
b For nonlinear DAC without correction
c For nonlinear DAC with proposed correction
d With correction, but using $NLF(z) = -1$
– – – $f_B = f_S/8$, inband limit for OSR = 4

The computed spectrum of the system operating with an ideal DAC but with nonideal opamps and capacitors (described above) is shown in Fig. 2*a*. Fig. 2*b* shows the spectrum using the nonlinear DAC without error correction. Large harmonics are generated and the spur-free dynamic range (SFDR) is only 52dB. Fig. 2*c* shows the result when using the digital correction described in this Letter; an SFDR > 100dB was achieved. To obtain sufficiently accurate estimates of e_D needed for such a high SFDR, DS_2 processed 2^{18} samples for each level of the DAC (a complete background calibration cycle then needs about 4s if DS_2 is clocked with f_S = 5MHz). Finally, Fig. 2*d* shows the detrimental effect of using $NLF(z) = -1$ (as carried out in earlier work [1, 3]), the drop in the SFDR being from 101 to 60dB.

Conclusions: An on-line digital correction method was proposed for ΔΣ ADCs with multibit internal quantisers. It is applicable even for ADCs with very low oversampling ratios, where the commonly used mismatch-shaping techniques become less effective. Simulations indicate that excellent linearity can be obtained using the proposed process.

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Reconfigurable phase-locked loops on FPGA utilising intrinsic synchronisability

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A new digital phase-locked loop (PLL), utilising the intrinsic synchronisability of electrical oscillators, on a field-programmable gate array has been developed. By interconnecting such PLLs, a dynamically reconfigurable clock network was formed, which has been difficult with conventional PLL techniques.

Introduction: Digital LSIs have generally been based on a synchronous scheme in which a global clock signal is distributed throughout the chip. However, circuit size and clock frequencies are increasing, therefore it is harder to distribute the clock signal (hereafter 'the clock') within an allowable phase delay. Asynchronous circuit design or locally synchronous circuits is a reasonable way to avoid this difficulty. Clock networks using distributed voltage-controlled oscillators [1, 2] can also be used. In contrast to these designs, we have developed a new digital phase-locked loop (PLL) which was tested on a field-programmable gate array (FPGA). This PLL utilises intrinsic synchronisability of electrical oscillators, and it can be simply implemented on an FPGA. It can provide dynamically reconfigurable clock networks, which have not been realised by conventional PLL techniques.

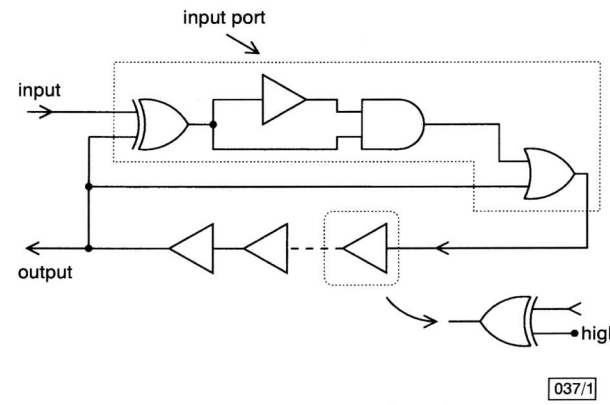

Fig. 1 *Impulse generating PLL (IPLL) with single input and output*

Impulse generating PLL (IPLL): Experimental results on the distributed clock oscillators for high-performance circuits show they have some advantages over conventional (H-tree like) clock networks [1, 2]. Such distributed oscillators are based on the conventional PLLs and require analogue elements in the circuits. We

have developed a new, reconfigurable PLL circuit (on an FPGA) which provides internal clock synchronisation. Fig. 1 shows the simplest configuration of this IPLL for a single input and output. (For multiple inputs and outputs, the same circuit can be obtained simply by adding the input ports.) The external clock is supplied at the input node. The internal clock is generated in the loop of the inverter array and the OR-gate. The input port consists of a phase comparison part (EXOR-gate) and a pulse generator (PG: inverter and AND-gate). This circuit does not require an analogue element (such as 'control voltage') and can be easily implemented on an FPGA.

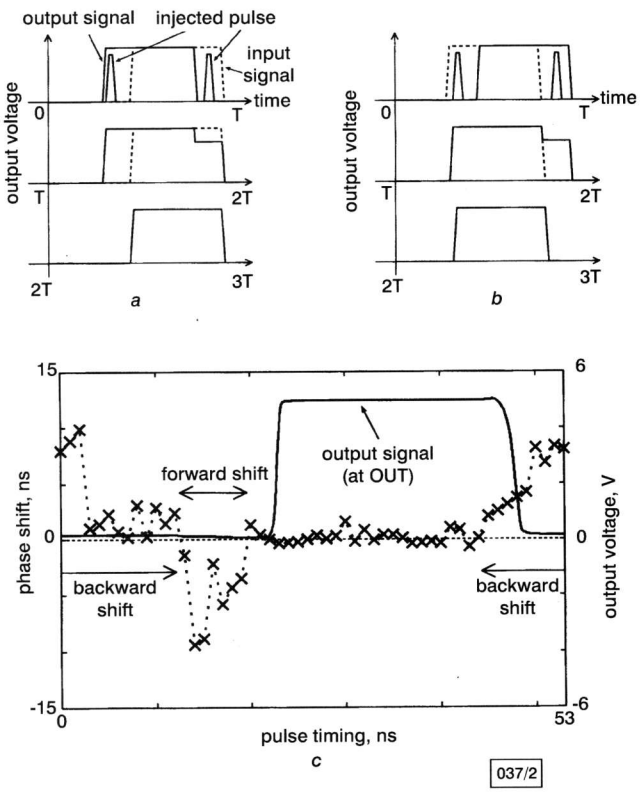

Fig. 2 *Synchronisation process*

a Forward shift
b Backward shift
c ISF

Synchronisability of single IPLL: It is known that the intrinsic nonlinear nature of electrical oscillators provides a robust oscillation in the waveform and frequency (which is useful for clock generation). This nonlinearity, on the other hand, produces a phase shift (which is sensitive to the timing of the perturbation) in the oscillation. This timing sensitive phase shift can be characterised as an impulse sensitive function (ISF) [3], which defines the phase shift as a function of the timing of the impulse injection to the circuit. The ISF was originally devised for jitter analysis, but here we use it for the synchronisability analysis of the IPLL as follows.

In the IPLL, if the input signal and output signal are synchronised (with no lag), the pulse generator (PG) outputs no impulse and the oscillation in the loop is not perturbed. Conversely, if there is a phase difference between the input and output signals, the PG is activated by the signal from the EXOR-gate. The timing of the impulse generation depends on the phase of the input (with respect to the output phase). Figs. 2*a* and *b* show the advanced and retarded input phase, respectively. In both cases, the output phase is entrained to the input phase (after a few cycles). In this particular IPLL, the size of the impulse (from the PG) is fixed, but the timing can be varied. The ISF can thus be directly measured by injecting this (fixed size) impulse externally at the node of the (disabled) PG output, with the input node being connected to the output node. In this way, the ISF is obtained as in Fig. 2*c* for one cycle of the oscillation. It is clear that the output signal phase is shifted backward (forward) if the impulse is applied after the falling edge (before the rising edge) of the output signal (see Figs. 2*a* and *b*). Thus, the only stable state is the synchronised state (with no lag), which is blocked with the forward shift and backward shift regions in the ISF. The fast acquisition shown in Figs. 2*a* and *b* is considered to be due to the direct phase shift which does not require the control voltage in conventional PLLs. We have therefore shown how a single IPLL utilises the intrinsic synchronisability in electrical oscillators that comes from their analogue nature. Next, we study the mutual synchronisation of interconnected IPLLs.

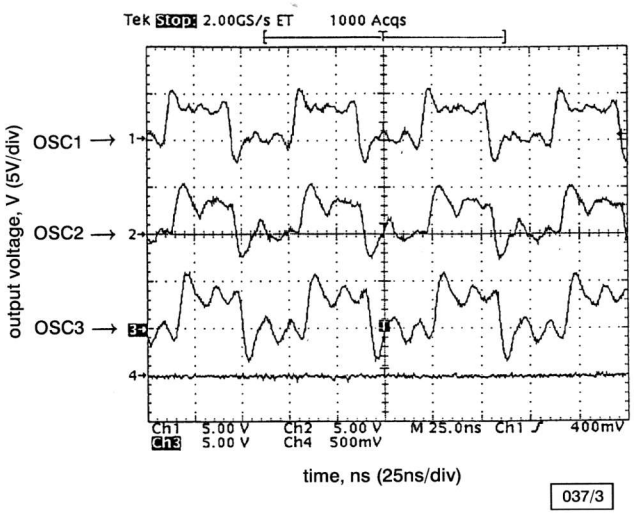

Fig. 3 *Output waveforms from unidirectory loop of three IPLLs (with 31-stage EXOR-gate arrays)*

Mutual synchronisation of IPLLs: We verified the mutual synchronisation ability of networks of IPLLs in the simplest configuration, i.e. three IPLLs interconnected in a (unidirectory) single loop where each IPLL outputs to the input port of the next IPLL and no external clock is required. Fig. 3 shows the output waveform from each IPLL (OSC1, OSC2, and OSC3); the rising and falling edges are sharp and the mutual synchronisation is robust (with small phase lags). From simulations with HSPICE, we found this small phase lag is an effect from the internal delay of each IPLL rather than from the signal delay between IPLLs. Larger networks of triangular or square lattices with IPLLs (each having two inputs and two outputs) were also studied with HSPICE and robust synchronisation was observed. However, in non-uniform large networks on an FPGA a long signal delay between some adjacent IPLLs makes the system beyond the synchronisability of each IPLL. Thus, a uniform layout of IPLLs that avoids a long signal delay is required for large networks. Larger networks of IPLLs are currently being developed.

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